







18. A chip-scale package as in claim 2, wherein said encapsulating material comprises a material having a low modulus of elasticity.

19. (Previously Amended) A chip-scale package as in claim 2, wherein each conductive carrier bond of said plurality of conductive carrier bonds further comprises an upper portion and a lower portion, said lower portion of a conductive carrier bond attached to the upper surface of a conductive trace of said plurality of conductive traces.

20. (Previously Amended) A chip-scale package as in claim 19, wherein said encapsulating material is disposed about the lower portions of said plurality of conductive carrier bonds.